Amendments to the Claims

The following claims listing shall supersede all previous listings filed in this application.

Claims Listing

1. (Currently Amended) A method of forming a metal interconnect in an opening formed on a substrate, comprising:

(a) providing a substrate with an opening formed therein~~, said opening has sidewalls, a top, and a bottom~~;

(b) forming a seed layer within said opening;

(c) forming a first metal layer on said seed layer by a first electrochemical plating (ECP) process to partially fill said opening;

(d) performing a first anneal step;

(e) forming a second metal layer on said first metal layer with a second ECP process to fill said opening; and

(f) performing a second anneal step;

wherein the first ECP process is performed using a first current density and the second ECP process is performed using a second current density, the first and second current densities being unequal.

2. (Original) The method of claim 1 further comprised of a cleaning process between steps (c) and (d) and between steps (e) and (f).

3. (Original) The method of claim 1 further comprised of forming a diffusion barrier layer on the sidewalls and bottom of said opening prior to forming a seed layer.

4. (Original) The method of claim 3 wherein said diffusion barrier layer has a thickness of about 200 to 500 Angstroms and is comprised of one or more of Ta, TaN, Ti, TiN, TaSiN, W, and WN.

5. (Currently Amended) The method of claim 1 wherein said first metal layer is copper and the seed layer is comprised of copper with a thickness between about 1000 and 2000 Angstroms.

6. (Original) The method of claim 1 wherein said first ECP process is performed at a temperature between about 10°C to 20°C and with a current density of about 5 to 15 mA/cm^2.

7. (Original) The method of claim 1 wherein said first and second anneal steps are performed in a process chamber at a temperature between about 180°C and 260°C for a period of about 10 to 200 seconds in a reducing gas or inert gas environment.

8. (Original) The method of claim 7 wherein the reducing gas is H_2 or NH_3.

9. (Original) The method of claim 1 wherein said first anneal step is performed in a PECVD process chamber with a H_2 plasma treatment comprised of a H_2 flow rate between about 5 and 10 sccm, a RF power of about 200 to 400 Watts, a chamber pressure of about 0.1 to 10 Torr, and a chamber temperature from about 150°C to 350°C for a period of about 10 to 200 seconds.

10. (Original) The method of claim 1 wherein said second anneal step is performed in a PECVD process chamber with a H_2 plasma treatment comprised of a H_2 flow rate between about 1 and 10 sccm, a RF power of about 300 to 400 Watts, a chamber pressure of about 0.1 to 10 mTorr, and a chamber temperature from about 150°C to 400°C for a period of about 10 to 200 seconds.

11. (Original) The method of claim 1 wherein the second ECP process is comprised of a first deposition step having a current density of 20 to 60 mA/cm^2 and a second deposition step having a current density of about 60 to 100 mA/cm^2.

12. (Original) The method of claim 11 wherein said first deposition step has a current density of about 40 mA/cm^2 and is used to fill said opening and wherein the second deposition step has a current density of about 60 mA/cm^2 and overfills said opening.

13. (Currently Amended) The method of claim 1 further comprised of a CMP process following said second anneal wherein said second metal layer becomes coplanar with ~~the~~ <u>a</u> top of the opening.

14. (Currently Amended) A method of forming a copper interconnect in an opening formed in a stack of dielectric layers on a substrate, comprising:

(a) providing a substrate with a stack of dielectric layers formed thereon;

(b) forming an opening comprised of a via and an overlying trench in said stack of dielectric layers, said via and trench each having sidewalls, a top, and a bottom;

(c) depositing a conformal diffusion barrier layer on the sidewalls and bottoms of said via and trench and depositing a seed layer on the diffusion barrier layer;

(d) depositing a first copper layer on the seed layer by a first electrochemical plating (ECP) process that fills said via and partially fills said trench;

(e) performing a first anneal step;

(f) depositing a second copper layer on said first copper layer with a second ECP process, said second copper layer fills said trench;

(g) performing a second anneal step; and

(h) planarizing said second copper layer to be coplanar with the top of the stack of dielectric layers;

wherein the first ECP process fills the via and about half of the trench.

15. (Original) The method of claim 14 further comprised of a cleaning process between steps (d) and (e) and between steps (f) and (g).

16. (Original) The method of claim 14 wherein said diffusion barrier layer has a thickness of about 200 to 500 Angstroms and is comprised of one or more of Ta, TaN, Ti, TiN, TaSiN, W, and WN.

17. (Original) The method of claim 14 wherein said seed layer is comprised of copper and has a thickness between about 1000 and 2000 Angstroms.

18. (Original) The method of claim 14 wherein the distance from the top of the trench to the bottom of the via is about 4000 to 13000 Angstroms.

19. (Cancelled)

20. (Original) The method of claim 14 wherein said first ECP process is performed at a temperature of about 10°C to 20°C and with a current density of about 5 to 15 mA/cm^2.

21. (Original) The method of claim 14 wherein the first and second ECP processes are performed in the same work piece and include an electrolyte solution comprised of $CUSO_4$, HCl, and one or more organic additives.

22. (Original) The method of claim 14 wherein said first and second anneal steps are performed in a process chamber at a temperature between about 180°C and 260°C for a period of about 10 to 200 seconds in a H_2, NH_3, or inert gas environment.

23. (Original) The method of claim 14 wherein said first anneal step is performed in a PECVD process chamber with a H_2 plasma treatment comprised of a H_2 flow rate between about 5 and 10 sccm, a RF power of about 200 to 400 Watts, a chamber pressure of about 0.1 to 10 Torr, and a chamber temperature from about 150°C to 300°C for a period of about 10 to 200 seconds.

24. (Original) The method of claim 14 wherein said second anneal step is performed in a PECVD process chamber with a H_2 plasma treatment comprised of a H_2 flow rate between about 1 and 10 sccm, a RF power of about 300 to 400 Watts, a chamber pressure of about 0.1 to 10 mTorr, and a chamber temperature from about 150°C to 400°C for a period of about 10 to 200 seconds.

25. (Original) The method of claim 14 wherein the second ECP process is comprised of a first deposition step having a current density of 20 to 60 mA/cm^2 and a second deposition step having a current density of about 60 to 100 mA/cm^2.

26. (Original) The method of claim 25 wherein said first deposition step has a current density of about 40 mA/cm^2 and is used to fill the trench and wherein the second deposition step has a current density of about 60 mA/cm^2 and is used to overfill the trench.

27. (Original) The method of claim 14 wherein planarizing said second copper layer involves a chemical mechanical polish process.

28. The method of claim 14 further comprised of a third ECP process followed by a third anneal step after the second anneal step and before said planarizing step.

29. (Original) The method of claim 28 wherein the second ECP process is performed with a current density of about 40 mA/cm^2 and the third ECP process deposits a third copper layer on the second copper layer and is performed with a current density of about 60 mA/cm^2.

30. (Original) A method of forming a dual damascene structure, comprising:

(a) providing a substrate with a stack of dielectric layers formed thereon;

(b) forming an opening comprised of a via and an overlying trench in said stack of dielectric layers, said via and trench each having sidewalls, a top, and a bottom;

(c) depositing a conformal diffusion barrier layer on the sidewalls and bottoms of said via and trench and depositing a seed layer on the diffusion barrier layer;

(d) depositing a first copper layer by a first electrochemical plating (ECP) process that fills said via and partially fills said trench;

(e) performing a first anneal step;

(f) depositing a second copper layer on said first copper layer with a second ECP process, said second copper layer fills said trench;

(g) performing a second anneal step;

(h) depositing a third copper layer on said second copper layer with a third ECP process, said third copper layer overfills said trench; and

(i) performing a third anneal step.

31-39 (Cancelled)

40. (New) The method of claim 30, wherein the first ECP process fills the via and about half of the trench.

41. (New) The method of claim 30, wherein said first ECP process has a first current density and said second ECP process has a second current density, the first current density being smaller than said second current density.

43. (New) The method of claim 30, wherein at least one of said first, second and third anneal steps comprises a PECVD process.

44. (New) The method of claim 30, wherein at least one of said first, second and third anneal steps comprises heating in a reducing gas or inert gas environment at about 180°C to about 260°C.

46. (New) The method of claim 30, wherein the first anneal step increases a grain size in the first copper layer.

47. (New) The method of claim 30, wherein the second anneal step increases a grain size in the second copper layer.

48. (New) The method of claim 30, further comprising the step of polishing the third copper layer and the second copper layer until the second copper layer is coplanar with a top surface of said stack of dielectric layers.

49. (New) The method of claim 48, wherein the step of polishing the third copper layer and the second copper layer removes the entire third copper layer.